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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,728	02/06/2004	Jingang Wu	021653-004200US	8605

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 07/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,728	WU ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Amendment filed on 5/2/2005.

Currently, claims 1-21 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being obvious over Narayan et al. (U.S. Patent No. 4,181,538 dated 1/1/1980) in view of Wu et al. (U.S. Publication No. 2005/0124080 filed 12/19/2003) and Wack et al. (U.S. Patent No. 6,818,459 filed 10/22/2003).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Narayan shows the method as substantially claimed and corresponding text as: providing a monitor wafer, the monitor wafer comprising a silicon material (col. 4, line 37); introducing a plurality of particles within a depth of the silicon material (col. 12, lines 22-25); introducing a plurality of dopant particles into a selected depth of the silicon material using an implantation tool (col. 4, lines 43-50), the amorphous state trapping the dopant particles (col. 4, lines 43-50); subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant (col. 4, lines 59-61); removing the monitor wafer measuring a sheet resistivity of

a surface region including the implanted dopant particles of the monitor wafer (col. 4, lines 62-66); determining a dose of the dopant bearing impurities (col. 6, lines 36-50) (claim 1). Narayan teaches that the monitor wafer is substantially free of screen oxide overlying a surface of the monitor wafer (col. 3, lines 55-60) (claim 2). Narayan teaches that the dopant particles are boron bearing impurities (col. 4, lines 44-47) (claim 5). Narayan shows the method as substantially claimed and corresponding text as: providing a monitor wafer, the monitor wafer comprising a crystalline Material (col. 4, line 37); introducing a plurality of particles within a depth of the material (col. 12, lines 22-25), introducing a plurality of dopant particles into a selected depth of the crystalline material using an implantation tool (col. 4, lines 43-50); subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant (col. 4, lines 59-61); removing the monitor wafer, measuring a sheet resistivity of a surface region including the implanted dopant particles of the monitor wafer (col. 4, lines 62-66); determining a dose of the dopant bearing impurities (col. 6, lines 36-50) (claim 13). Narayan teaches that the crystalline material comprises silicon (col. 4, line 36) (claim 14). Narayan teaches that the dose of the dopant bearing impurities is determined using a relationship between resistivity values and dose values (Table I) (claim 15). Narayan teaches that the relationship has been provided in a spatial plot (Table I) (claim 16). Narayan teaches that the dopant bearing impurities comprises boron species (col. 4, lines 44-50) (claim 18). Narayan teaches that the monitor wafer is substantially free from an overlying oxide layer before introducing the

dopant bearing impurities (col. 3, lines 55-60) (claim 19). Narayan teaches that the monitor wafer is a silicon wafer (col. 4, line 37) (claim 20).

Narayan lacks anticipation only in not explicitly teaching that: 1) the plurality of particles cause the silicon material to be in an amorphous state (claim 1); 2) the plurality of particles are silicon bearing species (claim 3); 3) the thermal anneal process is an RTP process at about 700 Degrees Celsius (claim 7); 4) the thermal anneal process is an RTP process at about 650 to 700 Degrees Celsius (claim 8); 5) the thermal anneal process is a rapid thermal anneal process (claim 9); 6) the operating of the production wafers occurs for 24 hours after determining the dose of the dopant impurities (claim 11); 7) the thermal anneal process also recrystallizes a portion of the amorphous silicon (claim 12); 8) the plurality of particles cause the crystalline material to be in an amorphous state; ...in the amorphous state using an implantation tool, the amorphous state trapping the dopant particles; (claim 13); and 9) the plurality of particles are silicon bearing species (claim 17).

Wu shows the monitoring low temperature rapid thermal anneal process using implanted wafers. In Fig. 2, the method introduces a plurality of particles (silicon-bearing particles) to cause an amorphous state within the monitor wafer [0045]. The wafer is then subjected to a rapid thermal process at about 650 to 700 degrees C. [0056]. Wu also shows the changing of monitor wafers daily [0008]. Some advantages of the method are an easy to use process that relies upon conventional technology, and provides higher device yields in dies per wafer [0013].

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Narayan, so that the monitor wafer can be placed in an amorphous state, as taught by Wu, with the motivation that, the process can be performed by conventional technology and provides higher device yields in dies per wafer.

Narayan as modified by Wu lacks anticipation only in not explicitly teaching: 1) operating the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor wafer is within a tolerance of a specification limit (claims 1 and 13); and 2) that the sheet resistivity is provided in a separate tool (claim 10).

Wack teaches a measurement and detection system for semiconductor processing that includes detecting defects, deposition material thickness, a sheet resistivity of a deposited material, a thermal diffusivity of a deposited material, or any combination thereof for the purpose of controlling the deposition process (bridging paragraph between col. 111 and col. 112).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Narayan as modified by Wu, in order to control the operation of an implantation tool, as taught by Wack, with the motivation that, Wack discloses a process for determining sheet resistivity with a separate tool.

Narayan as modified by Wu and Wack lacks anticipation only in not explicitly teaching that: 1) the silicon bearing species are implanted using a dose of $1x10^{15}$ atoms/cm^2 and an energy of 20KeV (claim 4); 2) the boron bearing impurities are implanted using a dose ranging from about $4x10^{14}$ through $1x10^{15}$ atoms/cm^2 and an

energy ranging from about 1-2 keV (claim 6); and 3) the one or more production wafers is characterized by shallow junction depth of less than about 40nm (claim 20).

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
July 7, 2005